REMARKS

The independent claims have been modified better to point out that which applicants regard as their invention and patentably to distinguish over the cited art.

The claims before the Examiner are claims 1 to 12; claim 12 has been withdrawn from consideration. It is noted that the Final Rejection mailed March 14, 2002 did not mention claim 12 even though that claim is pending. Applicants have not directed cancellation of that claim.

Claims 1, 3, 5, and 9 as revised each specify that (1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel and (2) each pixel is formed by a crossing region of the address electrode and the display electrode pair and that each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs; such a configuration is clearly shown in Figs. 2(B) and 3(B). Claim 7, because it is directed to a backplate only of the plasma display panel, does not refer to a pixel but does specify that each phosphor layer covers both the surface of the dark

dielectric layer and the surface of the ribs and that each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region of the ribs that corresponds to the region between the adjacent display electrode pairs.

Applicants respectfully submit that the claims as amended patentably define over Sasao et al. '860 alone or in combination with Ueoka et al. '349. A review of the drawings in the primary reference, particularly Fig. 1, shows no intermittent extension of the phosphor as claimed herein. The Sasao et al. '860 disclosure also has no mention of intermittent extension of each phosphor in the lengthwise direction of the ribs. The patent disclosure at column 3, lines 53 to 61, relate to coating phosphor layers on the dielectric layer upper surfaces and the adjoining rib wall surfaces. There is nothing suggesting that there is or should be intermittent extension of the phosphor layer in the lengthwise direction of the ribs so that no phosphor layer exists in the region on the ribs corresponding to the region between adjacent display electrode pairs. Applicants' invention, as explained in the specification at page 3 and other places helps deal with the problem of plasma display panel leakage to give high contrast and

sharpness and therefore represents an improvement over prior art systems. See also the discussion of the five advantages of the invention on pages 38 and 39.

Favorable treatment of the claims as amended is earnestly solicited.

If the only barrier to allowance is the presence of non-elected claim 12, the Examiner is authorized to cancel that claim for that express purpose. The Examiner is also asked to contact the undersigned should other changes be required in the application.

Respectfully submitted,

PARKHURST & WENDEL, L.L.P.

August 27, 2002
Date

Charles A. Wendel
Registration No. 24,453

CAW/ch

Attorney Docket No.: DAIN:496

PARKHURST & WENDEL, L.L.P.
1421 Prince Street, Suite 210
Alexandria, Virginia 22314-2805
Telephone: (703) 739-0220

Serial No. 09/287,190

CLAIM MARKUP

1. (Twice Amended) A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located between [the] adjacent linear ribs so that [they] the phosphor layers each extend intermittently in the lengthwise direction of the ribs for each pixel,

wherein (1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

3. (Twice Amended) A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a light-absorbing layer covering the address electrodes, and

linear ribs located between the address electrodes, with phosphor layers located between [the] adjacent linear ribs so that [they] the phosphor layers each extend intermittently in the

lengthwise direction of the ribs for each pixel,

wherein (1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

5. (Twice Amended) A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode comprising a transparent sustain electrode and a non-transparent metal bus electrode,

a translucent dielectric layer covering the display electrodes, and a magnesium oxide-containing, translucent protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dark dielectric layer covering the address electrodes,

linear ribs located between the address electrodes, and phosphor layers as so provided between [the] adjacent linear ribs so that a red-emitting phosphor layer, a blue-emitting phosphor layer and a green-emitting phosphor layer adjacent each other with a rib therebetween and these three different phosphor layers each extend intermittently in the lengthwise direction of the ribs,

wherein (1) each phosphor layer covers both the surface of the dielectric layer and the surface of the linear ribs within each pixel,

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair, and

(3) each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

7. (Twice Amended) A back plate for plasma display panels, which comprises;

a plurality of linear address electrodes on a glass substrate, a dark dielectric layer covering the address electrodes, and linear ribs between the address electrodes, and

phosphor layers located between [the] adjacent linear ribs so that a red-emitting phosphor layer, a blue-emitting phosphor layer and a green-emitting phosphor layer are adjacent each other with a rib therebetween and these three different phosphor layers each extend intermittently in the lengthwise direction of the ribs,

wherein (1) each phosphor layer covers both the surface of the dark dielectric layer and the surface of the ribs, and

(2) each phosphor extends intermittently in the lengthwise direction of the ribs so that the phosphor layer does not exist in the region on the ribs that corresponds to the region between the adjacent display electrode pairs.

9. (Twice Amended) A plasma display panel comprising;

a front plate and a back plate parallel to and facing each other having a space therebetween for a discharge gas,

plural pairs of display electrodes for surface discharge on the front plate parallel to each other, with each display electrode pair comprising a sustain electrode and a bus electrode,

a dielectric layer covering the display electrodes, and a protective film overlying the dielectric layer,

address electrodes on the back plate at right angles to the display electrode pairs, and a dielectric layer covering the address electrodes, and

linear ribs located between the address electrodes, with a phosphor layer located in each of a plurality of adjacent cell spaces formed by a plurality of adjacent linear ribs, said phosphor layers being intermittently interrupted so that they do not exist in the regions on the back plate [which] that correspond to the region between the adjacent display electrode pairs,

wherein (1) each phosphor layer covers the surface of the dielectric layer and the surface of the linear ribs within each pixel, and

(2) each pixel is formed by a crossing region of the address electrode and the display electrode pair.